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IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:

HIDEKI TAKAHASHI

: EXAMINER: LOKE, S.

SERIAL NO: 09/421,217

RCE FILED: FEBRUARY 7, 2002

: GROUP ART UNIT: 2811

FOR: INSULATED GATE SEMICONDUCTOR
DEVICE WITH LOW ON VOLTAGE AND
MANUFACTURING METHOD THEREOF

RECEIVED
MAY 21 2002
TECHNOLOGY CENTER 2800

RESPONSE

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

In response to the Office Action of February 28, 2002, please amend the above-identified application as follows:

IN THE CLAIMS

Please amend claim 22 to read as follows:¹

22. (Three Times Amended) An insulated gate semiconductor device, comprising:
a first semiconductor layer of a first conductivity type having first and second main
surfaces on opposite sides thereof;
a second semiconductor layer of a second conductivity type provided on said first
main surface of said first semiconductor layer;

figs. 3, 20, 23
Sub F
D/K
cont

¹A marked-up copy of the claim amendments is attached hereto.